**SISTEMAS DIGITALES AVANZADOS**

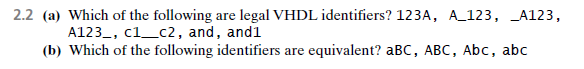
**Clave del curso: TE-2030**

**Nombre del Profesor: Juan M. Hinojosa Olivares**

**Nombre del alumno: Edison Altamirano**

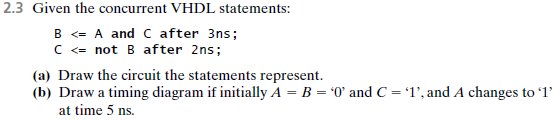
**Matricula: A00825234**

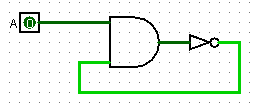
**Fecha de elaboración: 20/03/2020**

  
**A)**

|  |  |  |
| --- | --- | --- |
| Legal | Ilegal | |
| A\_123 | **123A** | Empieza con un numero |
| and1 | **\_A123** | Empieza con guion bajo |
|  | **A123\_** | Termina en guion bajo |
|  | **c1\_c2** | Guion bajo adyacente |
|  | **and** | Palabra reservada |

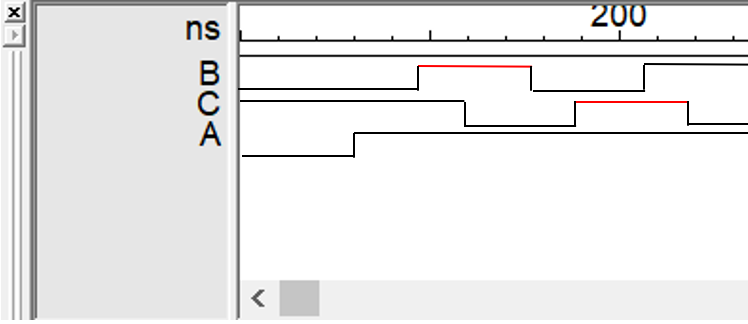
**B)** Todos son equivalente puesto que VHDL no es case sensitive.

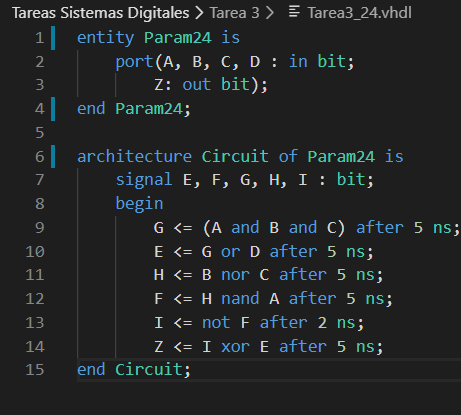
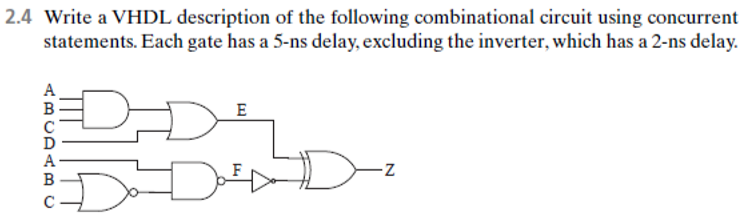
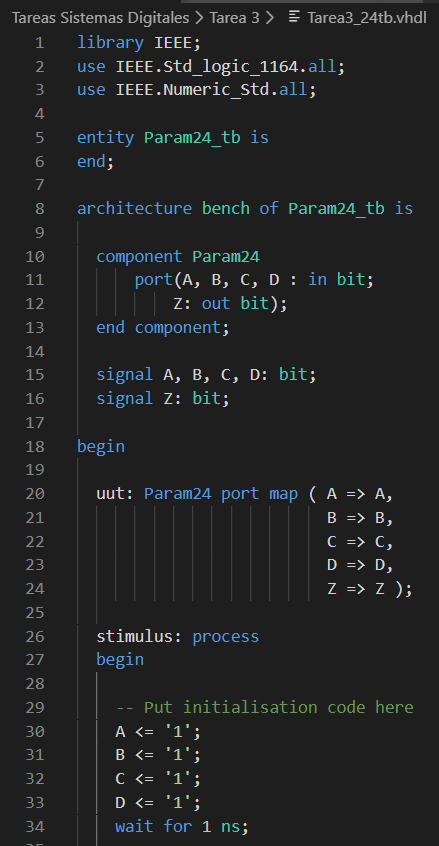


**a)**

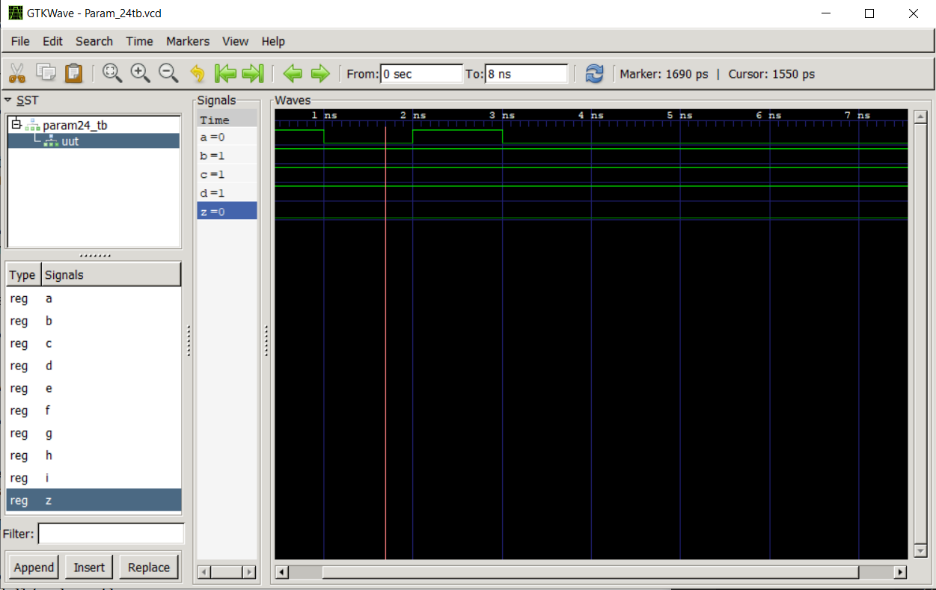
C

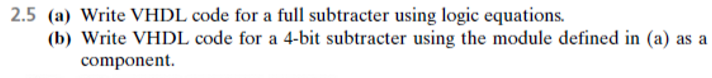
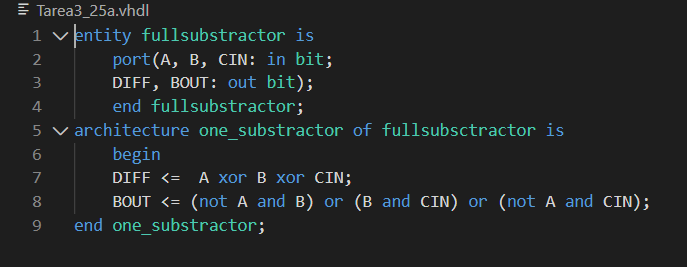
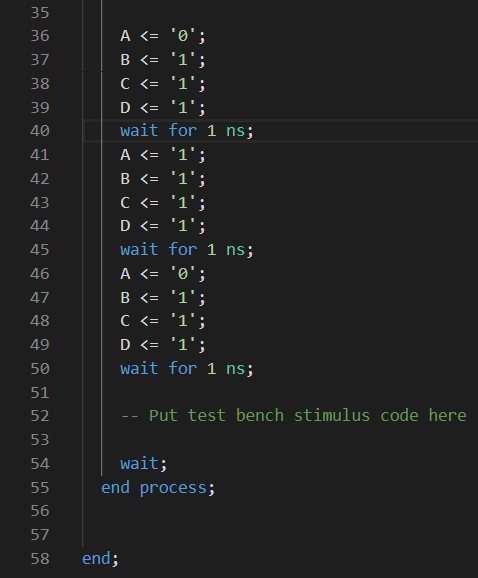
B

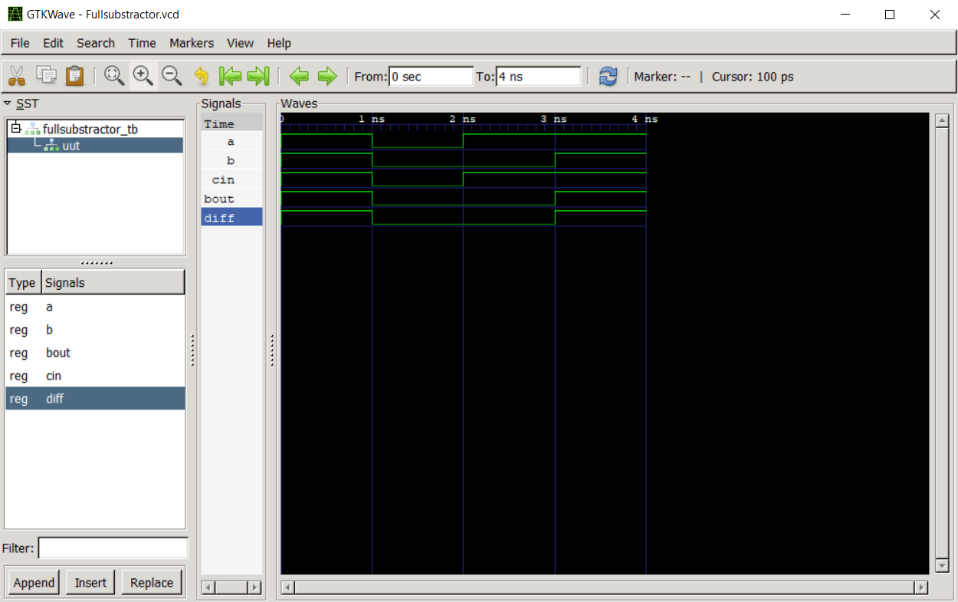
**b)**

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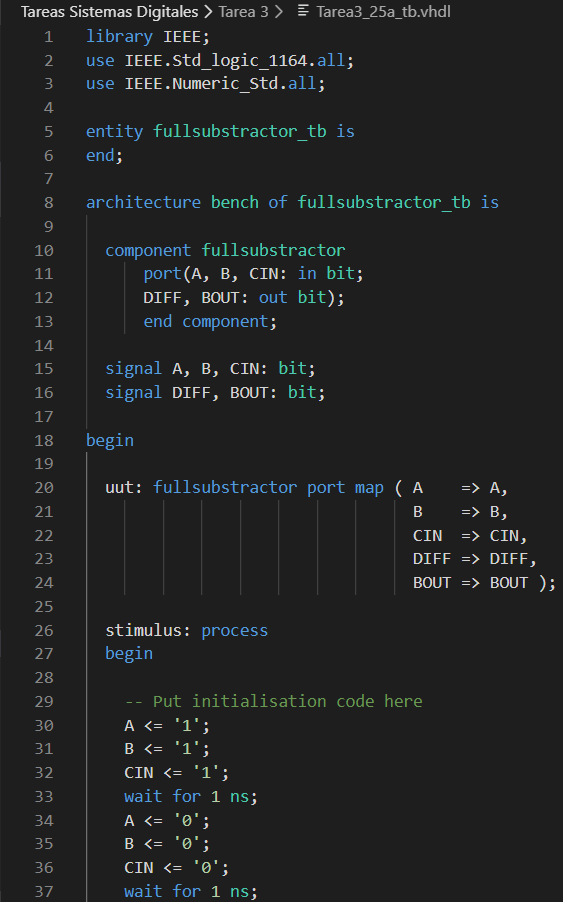
**Testbench para simulación**

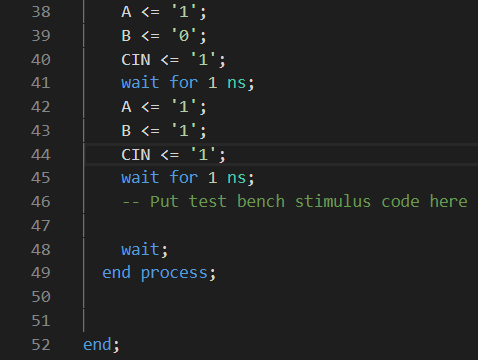
****

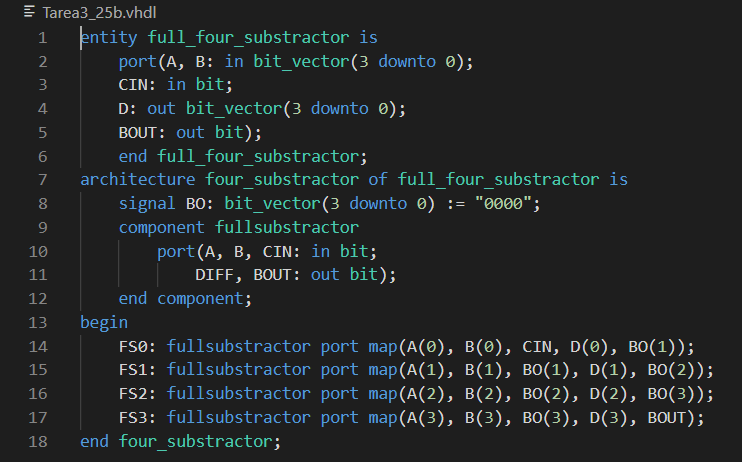
**a)**

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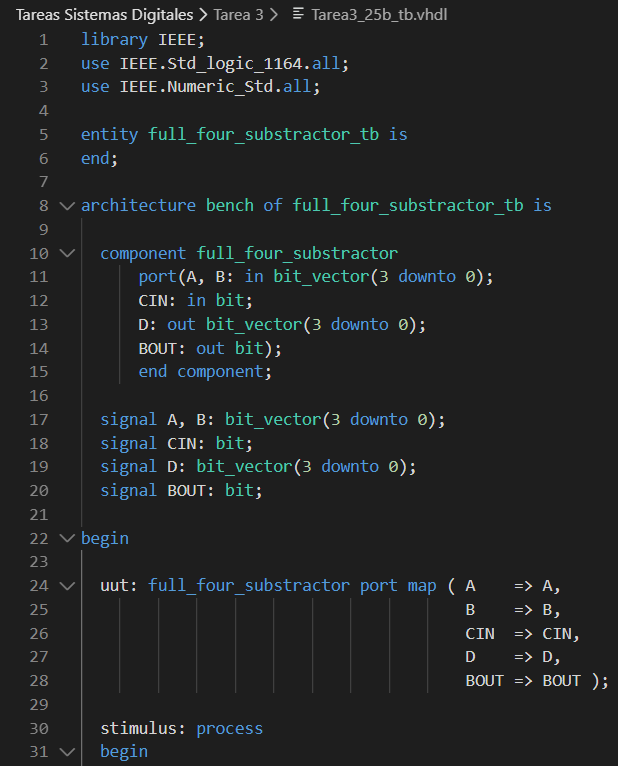
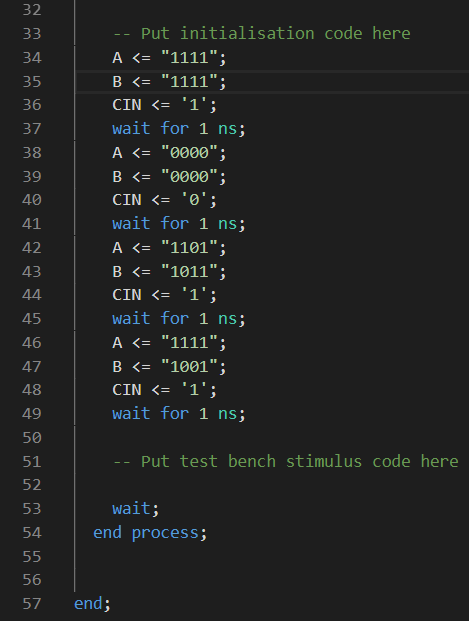
**Testbench para simulación**

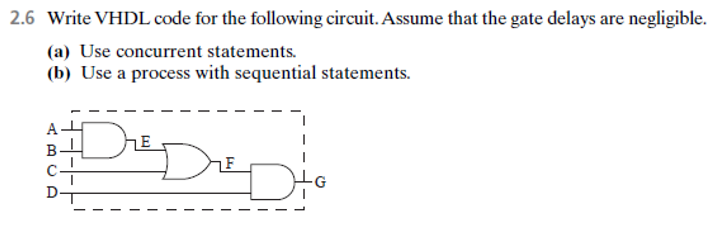
****

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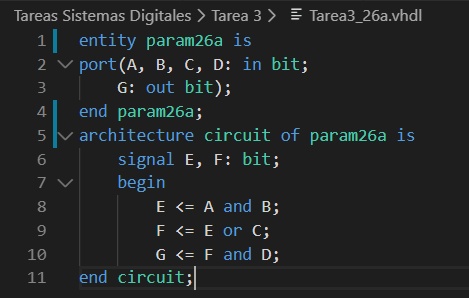
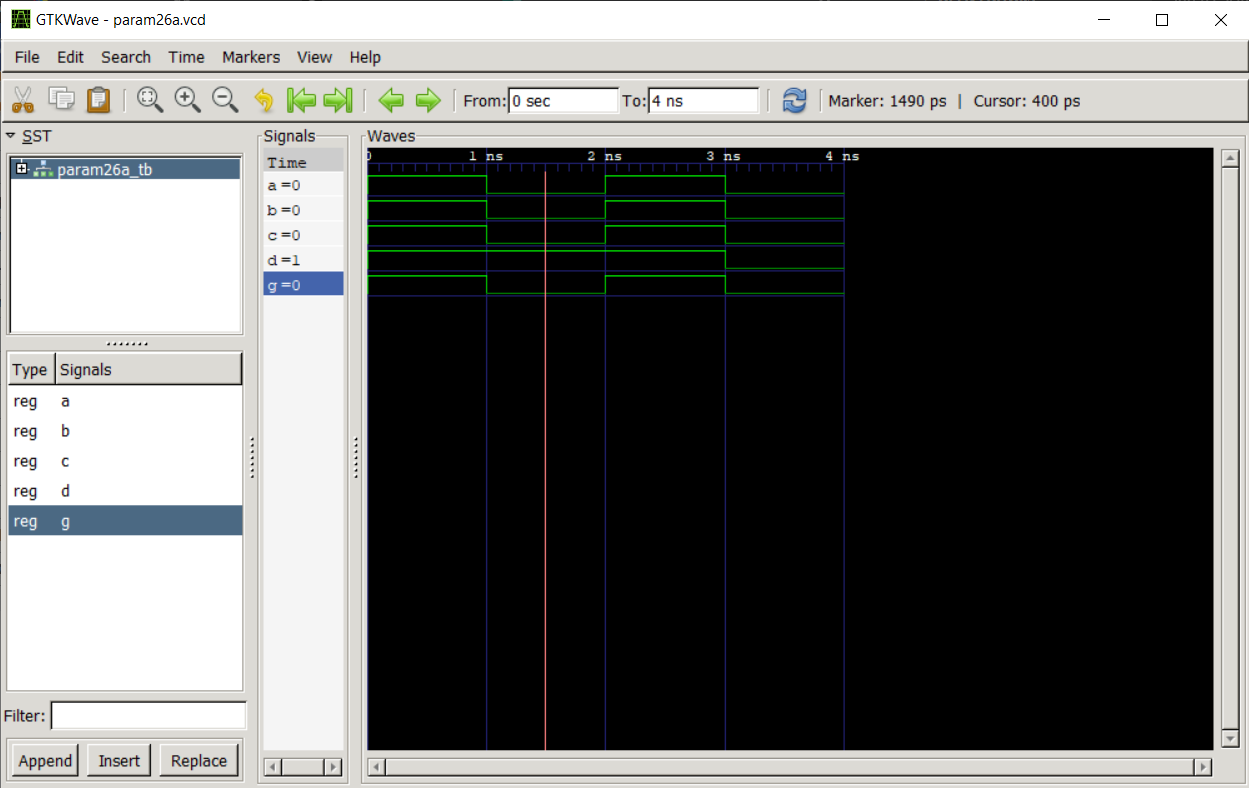
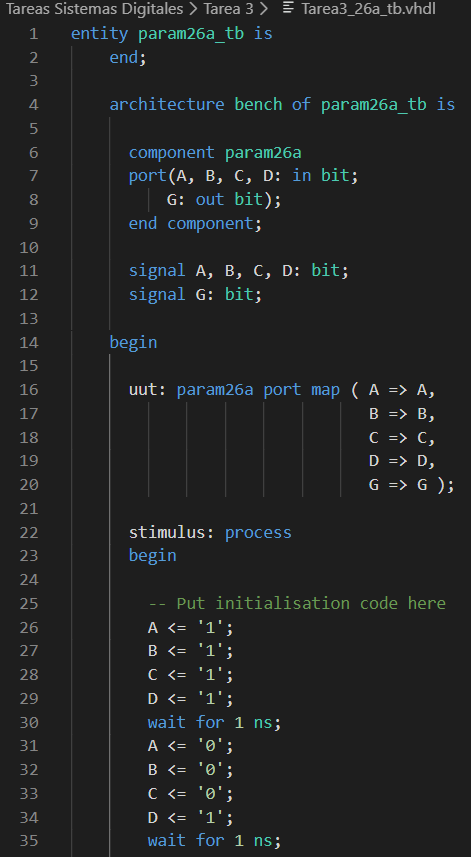
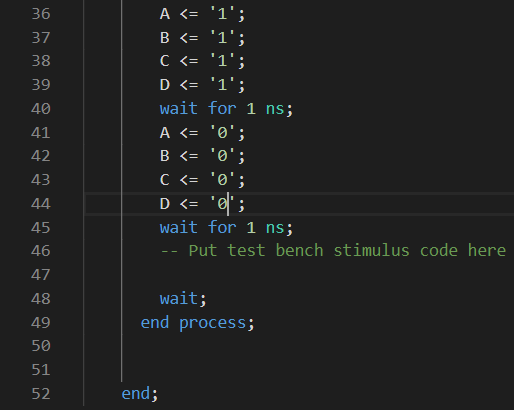
**b)**

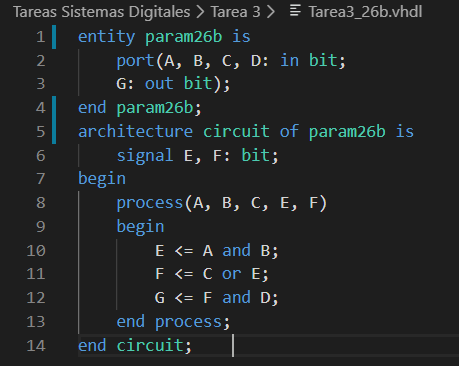
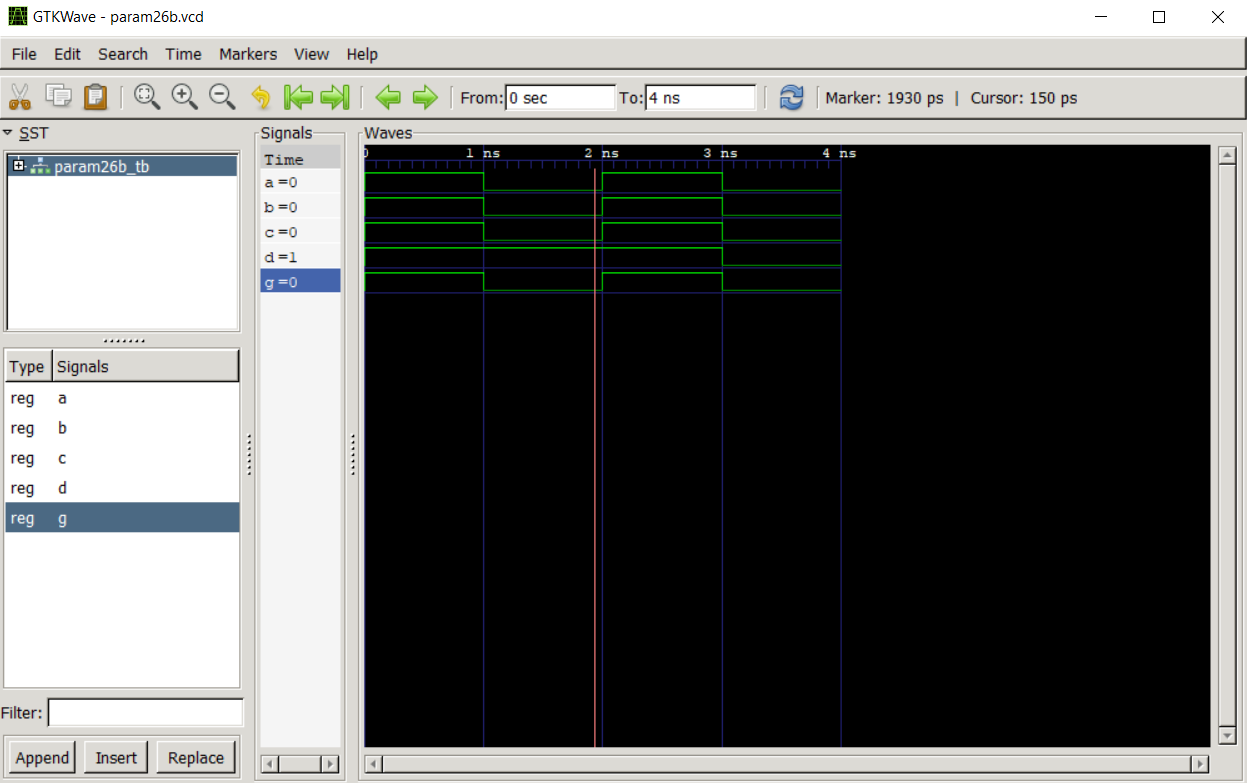
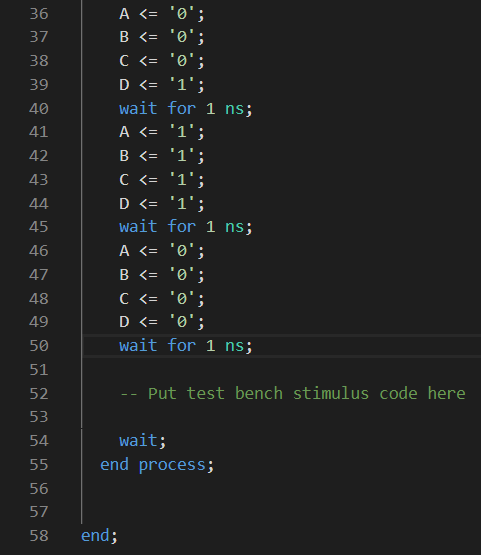
**Testbench para simulación**

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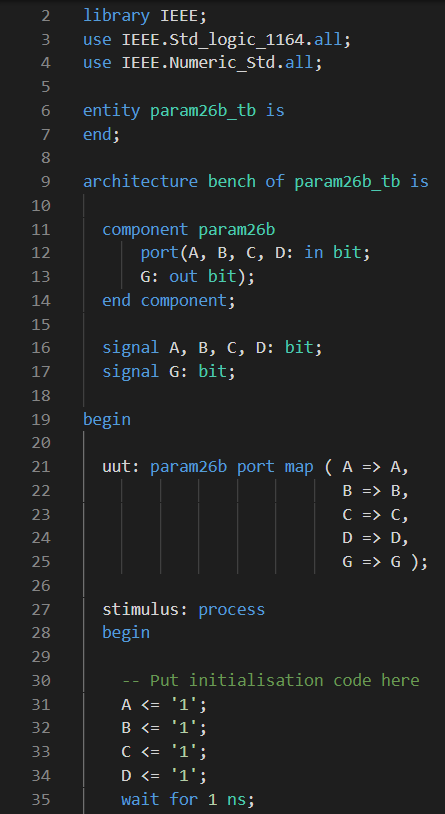
**a)**

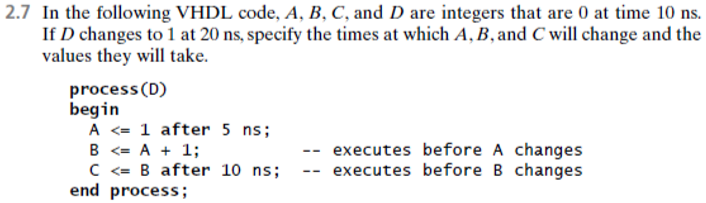
**Testbench para simulación**

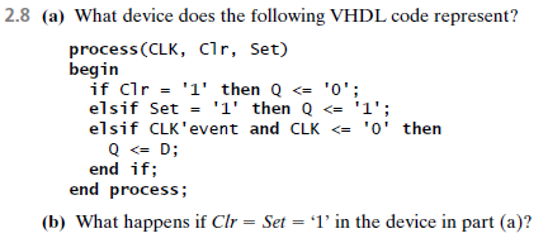
****

**b)**

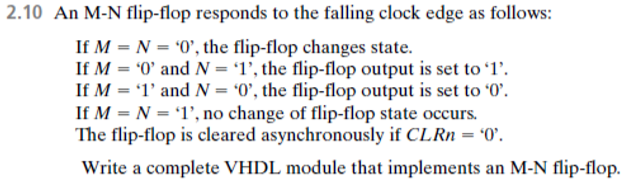
**Testbench para simulación**

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A cambia a 1 en 25 ns, B cambia a 1 en 20, y C no cambia.****

**A)** Flipflip D con salida activa asíncrono clear y set.

**B)** Q = ‘O’, porque Clear = 1 tiene prioridad.

